

Cont  
D1

12. (Twice Amended) A semiconductor device according to claim 14, wherein said transistor is a high voltage transistor having a source diffusion layer within said source side offset diffusion layer region and a drain diffusion layer within said drain side offset diffusion layer region and said source side offset diffusion layer and said drain side offset diffusion layer have impurity concentrations lower than those of said source diffusion layer and said drain diffusion layer.

---

D2

13. (Amended) A semiconductor device comprising:  
a source side offset diffusion layer region and a drain side offset diffusion layer region of a second conductivity type in a transistor formed, so as to be separated from each other, in a predetermined region in a region of a first conductivity type in a semiconductor substrate;

a gate insulator film formed between said source side offset diffusion layer region and said drain side offset diffusion layer region;

a gate electrode formed on said gate insulator film; and

a diffusion layer of the first conductivity type of which an impurity concentration is higher than that of said region of the first conductivity type and which is formed so as to surround said source side offset diffusion layer region, said drain side

offset diffusion layer region and said gate insulator film,  
wherein

both ends of said gate insulator film in a channel width direction form protruding portions that protrude at borders of said source side offset diffusion layer region and of said drain side offset diffusion layer region in a direction toward said diffusion layer of the first conductivity type so that said protruding portions of said gate insulator film make direct contact with said gate electrode, and wherein

said diffusion layer of the first conductivity type is formed so as not to be substantially present below said gate insulator film and is formed so as to be in contact with said protruding portions.

14. (Amended) A semiconductor device comprising:

a source side offset diffusion layer region and a drain side offset diffusion layer region of a second conductivity type in a transistor formed, so as to be separated from each other, in a predetermined region in a region of a first conductivity type in a semiconductor substrate;

a gate insulator film formed between said source side offset diffusion layer region and said drain side offset diffusion layer region;

a gate electrode formed on said gate insulator film; and  
a diffusion layer of the first conductivity type of which an impurity concentration is higher than that of said region of the first conductivity type and which is formed so as to surround said source side offset diffusion layer region, said drain side offset diffusion layer region and said gate insulator film, wherein

both ends of said gate insulator film in a channel width direction form protruding portions that protrude at borders of said source side offset diffusion layer region and of said drain side offset diffusion layer region in a direction toward said diffusion layer of the first conductivity type so that said protruding portions of said gate insulator film make direct contact with said gate electrode, and wherein

said diffusion layer of the first conductivity type is formed so as to surround said protruding portions and so as to be separated from the protruding portions by a predetermined distance.